

SAMSUNG Qualification Report

8GB eMMC

[FET-B 64Gb MLC NAND + Vincent Controller]

January, 2017

Memory Quality Assurance
Samsung Electronics Co., Ltd.

PQM170124002

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Revision	Date	Item	Description
Rev.00	January. 2017	-	First version

Contents

This report describes the reliability and qualification data for eMMC as follows,

1. General Information
2. Design & Process Information
3. Package Information
4. Reliability Test Result

- **Device (Component)**

Product	PKG Type	VDD		Temperature (operation)	Part No.
		eMMC			
		Interface Power	Memory Power		
8GB eMMC	153 FBGA	1.7V~1.95V or 2.7V~3.6V	2.7V ~ 3.6V	-25℃ ~ 85℃	KLM8G1GETF

Contents

This report describes the reliability and qualification data for eMMC as follows,

1. General Information

- Device**
- Pin Configuration**

2. Design & Process Information

3. Package Information

4. Reliability Test Result

- Pin Configuration For 153 FBGA (11.5 x 13)**

[Table 2] 153 Ball Information

Pin NO	Name
A3	DAT0
A4	DAT1
A5	DAT2
B2	DAT3
B3	DAT4
B4	DAT5
B5	DAT6
B6	DAT7
K5	RSTN
C6	VDD
M4	VDD
N4	VDD
P3	VDD
P5	VDD
E6	VDDF
F5	VDDF
J10	VDDF
K9	VDDF
C2	VDDI
M5	CMD
H5	Data Strobe
M6	CLK
J5	VSS
A6	VSS
C4	VSS
E7	VSS
G5	VSS
H10	VSS
K8	VSS
N2	VSS
N5	VSS
P4	VSS
P6	VSS

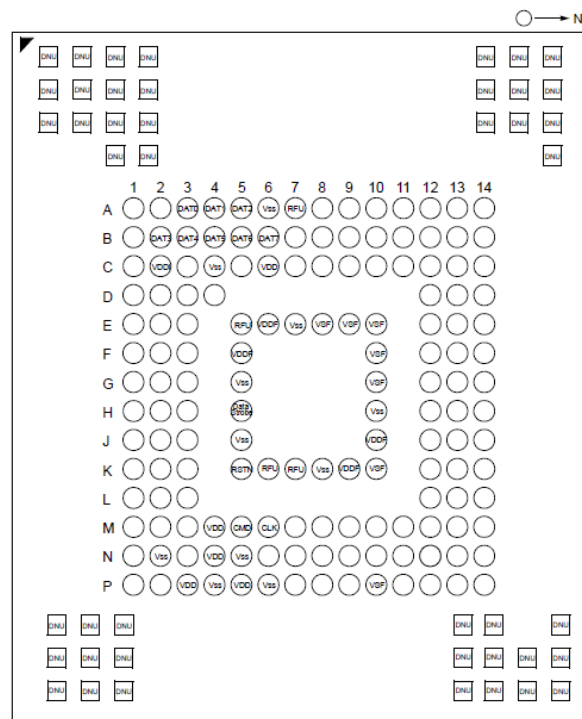


Figure 1. 153-FBGA

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■ Design

Die Revision	64Gb 2bit MLC	S4LL184X01(Vincent)
Die dimension	11.945mm x 5.9500mm	3.6850mm x 1.8540mm
Memory Cell Dimension	0.001086um ²	- SPSRAM, RA1_HD : 0.299um ² - RA2_HD, RA2_UHD : 0.576um ² - RF1_HD : 0.299um ²
Basic Design Rule	14.3nm	0.045um
Gate Dielectric Thickness	62+/-1Å	SG:18Å / DG:58Å
Memory Cell Type	Stacked Cell Structure	SRAM : 6T/8T Cell ROM : VIA ROM

■ Process

Die Revision	64Gb MLC NAND
Poly I	Poly Si
Poly II	Poly Si + Transistor Gate (WN/W)
Bit Line (Metal I)	Ta/Cu
Metal II	Ti/Al/TiN
Passivation	HDP + PE-SiN
Process Feature	2 Metal / 1 Poly

Die Revision	S4LL184X01 (Vincent)
Poly	Transistor Gate (NiSi2 + Poly Si)
Metal 1	TaN/Ta/Cu
Metal 2	TaN/Ta/Cu
Metal 3	TaN/Ta/Cu
Metal 4	TaN/Ta/Cu
Metal 5	TaN/Ta/Cu
Metal 6	TaN/Ta/Cu
Metal 7	TaN/Ta/Cu
Metal 8	TaN/Ta/Cu
Process Feature	1 Poly NiSi2 / 8 Metal

Contents

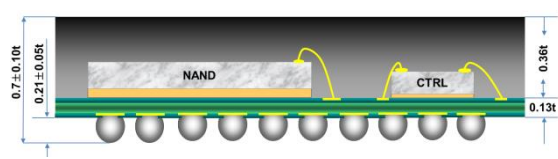
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1. General Information
2. Design & Process Information
- 3. Package Information**
 - Assembly Information**
4. Reliability Test Result

■ 153FBGA (11.5 x 13) – KLM8G1GETF

Item	8GB eMMC
PKG Type	153 FBGA
Lead Frame	PCB
EMC	Halogen Free
Wire	Au Wire
Adhesive Type	Film Type
Ball Material	Sn1.2Ag0.5Cu0.05Ni

■ 153FBGA (11.5 x 13) Vertical Structure – KLM8G1GETF

Item		Description	Dimension
Package Type		FBGA	
EMC		Halogen Free	
Solder Ball	Diameter	0.3mm (After Reflow : 0.32mm ±0.05)	
	Composition	LF Alloy	
Adhesive		Film Type	
Interconnection		Au Wire	

■ 153FBGA (11.5 x 13) – KLM8G1GETF

Product	8GB eMMC
PKG Size	11.5mm * 13.0mm
PKG Thickness	Max 0.8mm
Chip – 1 st	Vincent Controller
Chip – 2 nd	64Gb MLC NAND
Ball Diameter dimension	0.3mm
Ball Pitch	0.5mm (Typical)

Contents

This report describes the reliability and qualification data for eMMC as follows,

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4. Reliability Test Result

- **Assembly Qualification Test**

- **Package Level Reliability Test**

 - . **Environment, Characteristics Test**

 - . **Daily Amount Data Size, Data Retention, Operating Test**

 - . **Almighty , SQA ,Compatibility Test**

 - . **Product Dynamic Life Tests (FITs)**

■ Front End Process

Process	Item	Sample Size	Result	Criteria
Die Attach	Bond Line Thickness	22 Point / Lot	0/22	0/1
	Tape Void	1 Frame / 3Lot	0/1	
	Internal Visual Inspection	200 units / 3Lot	0/200	
Wire Bond	Bond Pull Test	25 wires / Lot	0/25	0/1
	Ball Height	11 balls / Lot	0/11	
	Internal Visual Inspection	200 units / Lot	0/200	
	Loop Height	11 units / Lot	0/11	

■ Back End Process

Process	Item	Sample Size	Result	Criteria
Mold	X-ray Inspection	1 Shot / Lot	0/1	0/1
	C-SAM Inspection	1 Frame / Lot	0/1	
	External Visual Inspection	3 Shot / Lot	0/3	
Solder Ball Attach & Reflow Cleaning	Solder Ball Shear Test	25 balls / unit / 3Lots	0/25	0/1
	External Visual Inspection	200 units / Lot	0/200	
Saw & Sorter	Package Out Dimension	11 units / 3Lots	0/11	0/1
	External Visual Inspection	200 units / Lots	0/200	

■ Environment Test Result

Item		condition	S/S	Number of Failure	
Pre-Condition (JEDEC Level 3)	HTS	150℃, No bias	116	168hr	300hr
				0	0
	LTS	-40℃, No bias	116	168hr	300hr
				0	0
	uHAST	130℃, 85%RH, 1atm	116	168hr	
				0	
	TC	- 55℃ ~ 125℃ Cycling	116	300cyc	600cyc
				0	0
	HTDR	85℃, 72hr	116	72hr	
				0	

Note) HTS,LTS,TC,uHAST and HTDR were done after Pre-condition.

Pre-Condition Test flow [JEDEC Level 3]

: Bake → T/C → Moisture Soak (L3) → IR Reflow 3Times @ pre-program state

Check the eMMC function after perform the environment test.

■ Characteristics Test Result

Classification	S/S	Condition	STD
Electro Static Discharge	40	HBM : 1000V Pass	Mil-STD 883E Method 3015.7 JESD A114
	30	CDM : 500V Pass	JESD 22 C101 EIAJ ED 4701~305
Latch-up	10	Power : 6V Pass	JESD 78
	40	Current : 150mA Pass	

■ The Daily Amount Data Size

eMMC Density	The Daily Amount Data Size
8GB	8 TBW @ during 5years

Note) Data Category : User Daily workload during 5 years

■ Data Retention Test Result

Test	Test Condition		S/S	User Retention Time	
				1 Year	5 Year
Data Retention	10% TBW	Ta=85°C	76	Pass	Pass
	100% TBW		76	Pass	-

Note) Data Category : Total Amount Data Size(TBW) = User Daily workload * 5 Year

■ Operating Test Result

Test Item	Condition	S/S	R168
HRT	85℃, Operating	76	0
LRT	-25℃, Operating	76	0
SRT	-20℃~60℃, Operating	76	0
POR	-20℃~60℃, Operating	45	0
Functionality	-20℃~60℃, Operating	45	0
Fault injection	25℃, Operating	45	0

Note) HRT : High temperature Reliability Test
 LRT : Low temperature Reliability Test
 SRT : Swing temperature Reliability Test
 POR : Power Off Recovery

■ Almighty Test Result

Test Item	Condition	S/S	Category	Test Case	Result
Almighty	25℃	5	Functionality	1805	PASS
			SPOR	70	
			Timeout	75	
			FMEA	99	
			Mode to Mode	230	
			TOTAL	2379	
AC/DC	-25℃/25℃/85℃	30	AC/DC		PASS

■ Software Qualification Test Result

Test Item	Condition	S/S	Result
Functionality	25℃	8	PASS (3088 ITEM)
R1	25℃	40	PASS (46 ITEM)
R2	25℃	30	PASS (153 ITEM)

■ Compatibility Test Result

Application		S/S	Result
Function Test	FMEA	2	PASS
	Pattern Test	2	PASS
	OS-less	2	PASS
Performance Test	User Scenario Test	2	PASS
	Bench Mark Tool Test	10	PASS
AVL Test	WHCK, CTS/GTS	2/2	PASS
SPOR	Stress + SPOR Time Scan	7	PASS
Stress Test	Worst Precondition, IO Pattern Test..	13	PASS
DC test		2	PASS

■ 3.3V Product Reliability FITs Prediction (60% Confidence Level)

Item	Condition	S/S	Number of Failure				
			96hr	168hr	300hr	500hr	1Khr
EFR	125`C, 3.3V Dynamic Stress	1000	0	0	-	-	-
IFR		387	-	-	0	0	0

- FIT = $[\text{Chi square } (2r+2) \times E9] / [2 \times \text{Device} \times \text{Hour} \times \text{AF}]$

Where , AF = $[\text{AFT} \times \text{AFV}]$

AFT = $\text{Exp} [\text{Ea}/K(1/\text{Ts} - 1/\text{Td})]$, Ea = 0.5eV, Ts = 125`C, Td = 55`C

AFV = $\text{Exp Beta} (\text{Vs} - \text{Vd})$, Beta = 3.2, Vs = 3.3V, Vd = 2.3V

Power Design Scheme ;

EVC Condition : Ext. VCC = 3.3V Int. VCC = 3.3V

USER Condition : Ext. VCC = 3.3V Int. VCC = 2.3V

> Fit of EFR : 9.93 Fits

> Fit of IFR : 4.31 Fits

■ Product Reliability FITs Prediction : S4LL180X01 (Vermont)

- FIT rate per 1000hours calculation
- Confidence level (CL) : 60% @ 55℃, $V_{DD} = 1.21V$
- Activation energy (E_a) : 0.7eV

$$FR = \frac{X^2 (2n+2, 60\%CL)}{2 * EDH(DH * AF)} \quad \times 10^9$$

Items	Conditions	Q'ty	# of failure	DH	AF_T	AF_V	AF (= $AF_T * AF_V$)
IFR	120 ℃, 1.31V Dynamic stress	231 ea	0	231000	171.2	1.49	255.4

- EDH : Equivalent device hours
- DH : Device hours
- n : number of failure

- AF : Acceleration factor ($AF_T * AF_V$)
- + AF_T : Temperature AF
- + AF_V : Voltage AF

- FIT of IFR : 15.5

Note) FIT (Failure In Time) is represented the number of failures expected per 10^9 hours at 55℃

Thank You!

